

# ADPCM VOICE SYNTHESIZER ROM-LESS ENHANCED *PowerSpeech*ä

### **GENERAL DESCRIPTION**

The W58100 is a CMOS IC that is used solely for the purpose of demonstrating the W581xx series enhanced *PowerSpeech*<sup>™</sup> products.

The W58100 employs the same JUMP-GO architecture as Winbond's other *PowerSpeech*<sup>™</sup> products. Unlike standard products, however, the W58100 does not include built-in memory, because the chip is designed to serve only as a demonstration chip for the W581xx series ICs. Hence the W58100 must be operated with an external memory device (e.g., a flash EPROM memory IC). The W58100's LOAD and JUMP commands and 8 programmable registers provide powerful user-programmable functions that make this chip suitable for a wide range of speech IC applications.

### FEATURES

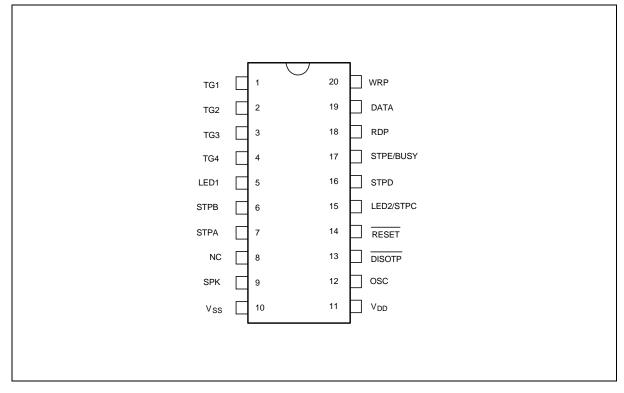
- Wide operating voltage range: 2.4 to 5.5 volts
- Serves as a demo chip for W581xx series products (no built-in ROM)
- Programmable speech synthesizer
- 4-bit ADPCM synthesis method and 8-bit D/A converter
- Maximum 4 trigger inputs
- · Fading effect (patent pending) control for each voice segment
- · Maximum two LEDs, and five STOP outputs
- Flexible functions programmable through the following:
  - LD (load), JP (jump) commands
  - 8 general registers: R0-R7
  - Three special registers: EN, STOP, and MODE
  - Conditional instructions
  - Speech equation
- · Programmable power-on initialization (POI), which can be interrupted by trigger inputs
- Interrupt or non-interrupt for rising or falling edge of each trigger pin (this feature determines retriggerable, non-retriggerable, overwrite, and non-overwrite features of each trigger pin)
- · LED On/Off control can be set independently in each GO instruction of speech equations
- Independent control of LED 1 and LED 2
- Total of 256 voice group entries available for programming (Including eight hardware and 248 software group entry points)
- CPU interface
- The following mask options are available:

# Preliminary W58100



- LED flash type: synchronous/alternate
- LED1 section-controlled: Yes/No
- LED2 section-controlled/STPC-controlled
- LED volume controlled: No/Yes
- Normal/CPU mode
- STPE or BUSY selection
- The following register controls are available:
  - Trigger input debounce time: Long/Short
  - Pin option for LED2/STPC
  - LED turn-on mode: Flash/DC

## **PIN CONFIGURATION**





## **PIN DESCRIPTION**

NO.	NAME	I/O	FUNCTION	
1	TG1	Ι	Trigger Input 1	
2	TG2	Η	Trigger Input 2	
3	TG3	Η	Trigger Input 3	
4	TG4	Ι	Trigger Input 4	
5	LED1	0	LED 1	
6	STPB	0	Stop signal B	
7	STPA	0	Stop signal A	
8	NC	-	Not connected	
9	SPK	0	Current output for driving an external speaker	
10	Vss	-	Negative power supply	
11	Vdd	-	Positive power supply	
12	OSC	Ι	Oscillation frequency control, connect Rosc to VDD	
13	DISOTP	Ι	Disable all of the serial interface pins (low active)	
14	RESET	Ι	Reset pin (low active)	
15	LED2/STPC	0	LED2 signal output or Stop C output	
16	STPD	0	Stop D output	
17	STPE/BUSY	0	Stop E or Busy signal output	
18	RDP	0	Read pulse clock output for serial interface	
19	DATA	I/O	Bidirectional Data Pin for the serial interface	
20	WRP	0	Write pulse clock output for serial interface	

#### **ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Power Supply	VDD-VSS	-	-0.3 to +7.0	V
Input Voltage	Vin	All Inputs	Vss -0.3 to VDD +0.3	V
Storage Temp. TSTG		-	-55 to +150	°C
Operating Temp. TOPR		-	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.



# **ELECTRICAL CHARACTERISTICS**

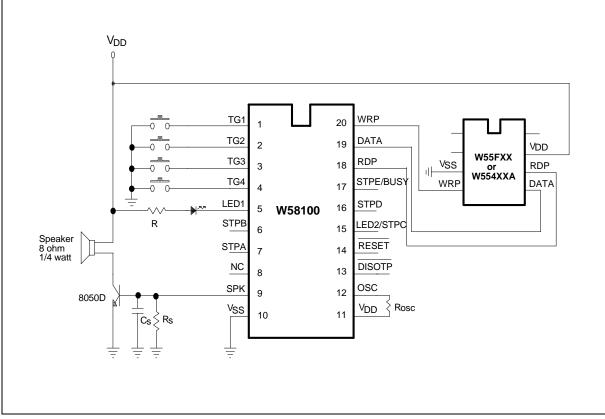
 $(T_A = 25^\circ C, V_{SS} = 0V)$ 

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Operating Voltage	Vdd	-	2.4	4.5	5.5	V
Input Voltage	VIL	-	Vss -0.3	-	0.3 Vdd	V
	Vін		0.7 Vdd	-	Vdd	
Standby Current	IDD	VDD = 5V, all I/O pins unconnected, no playing	-	-	1	μA
Operating Current	IOP1	VDD = 3V, No Load	-	-	400	μΑ
	IOP2	VDD = 5V, No Load	-	-	800	
Input Current for TG1–TG4 Pins	lin1	VDD = 3V, VIN = 0V	-	-	-6	μA
Input Current for DISOTP Pin	lin2	VDD = 3V, VIN = 0V	-	-	-6	μA
Input Current for RESET Pin	ling	VDD = 3V, VIN = 0V	-	-	-30	μΑ
SPK (D/A full scale)	lo	$VDD = 4.5V, RL = 100\Omega$	-4.0	-5.0	-6.0	mA
Output Current of	IOL1	VDD = 3V, VOUT = 1V	8	-	-	mA
LED1/2	IOL2	VDD = 4.5V, VOUT = 1V	12	-	-	
Output Current of	IOL	VDD = 3V, VIN = 0.4V	1	-	-	mA
STPA-STPE	Іон	VDD = 3V, VOUT = 2.6V	-1	-	-	
Oscillation Freq.	FOSC1	VDD = 5V, ROSC = Typ.	2.7	3	3.3	MHz
Osc. Freq. Deviation by Voltage Drop	AFosc Fosc	F(3.0V) – F(2.4V) F(3.0V)	-	4	7.5	%
Debounce Time.	TDEB1	Rosc = Typ., SR = 6 KHz	20	30	40	mS
	TDEB2	Rosc = Typ., SR = 6 KHz	166	250	332	μS

Rosc = Typ. = 1.2M ohm



# **TYPICAL APPLICATION CIRCUIT**



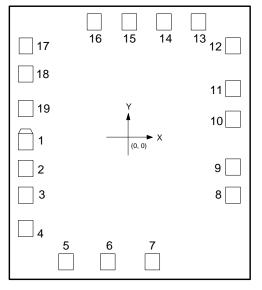
Notes:

1. In principle, the playing speed determined by Rosc should correspond to the sampling rate during the coding phase. However, the playing speed may be adjusted by varying Rosc.

- 2. Rs is an optional current-dividing resistor. If Rs is added, the resistance should be between 470 and 750.
- 3. R is used to limit the current on the LED.
- 4. Cs is optional.
- 5. The DC current gain  $\beta$  of transistor 8050 ranges from 120 to 200.
- 6. All unused trigger pins can be left open because of their internal pull-high resistance.
- 7. No warranty for production.



#### **BONDING PAD DIAGRAM**



PAD NO.	PAD NAME	
1	TG1	
2	TG2	
3	TG3	
4	TG4	
5	LED1	
6	STPB	
7	STPA	
8	SPK	
9	Vss	
10	Vdd	
11	OSC	
12	DISOTP	
13	RESET	
14	LED2/STPC	
15	STPD	
16	STPE/BUSY	
17	RDP	
18	DATA	
19	WRP	

Note: Substrate is tied to Vss.



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Note: All data and specifications are subject to change without notice.